

## **IN THE CLAIMS**

This listing of the claim will replace all prior versions and listings of claim in the present application.

### **Listing of Claims**

1. (currently amended) A storage unit comprising:
  - a channel control portion for receiving a data input/output request;
  - a cache memory for storing data;
  - a disk control portion for performing input/output processing on data in accordance with said data input/output request; and
  - a plurality of disk drives for storing data,  
wherein at least two of said disk drives input data to and output data from said disk control portion at different communication speeds, relative to the communication speeds of the others of said disk drives,  
a generation portion for generating a clock signal by using a pulse signal transferred for communication between said disk control portion and said disk drives;  
an identification portion for identifying a frequency of said pulse signal;  
a frequency division portion for dividing a frequency of said clock signal at a frequency division ratio that corresponds to a frequency of said pulse signal; and  
a synchronization portion for synchronizing said pulse signal with a clock signal having said divided frequency,  
wherein said identification portion comprises:  
a charge accumulation portion for outputting a voltage that corresponds to a quantity of charge accumulated therein,

a charge quantity variation portion for varying said quantity of said charge accumulated in said charge accumulation portion, at a certain variation rate,

a charge quantity variation suppression portion for inhibiting said variation only during a certain lapse of time each time a signal level of said pulse signal is switched,

a signal output portion for outputting a signal that corresponds to whether said voltage output from said charge accumulation portion satisfies a criterion,

a time measurement portion for measuring a lapse of time that has elapsed since said quantity of said charge accumulated in said charge accumulation portion started to vary, and

a frequency identification portion for identifying said frequency based on said lapse of time from a moment when said quantity of said charge started to vary to a moment when said signal that indicates that said voltage of said charge accumulation portion satisfies said criterion was output.

2. (currently amended) The storage unit according to claim 1, wherein said storage unit has a plurality of communication paths for connecting at least one of said disk drives in such a manner as to constitute a loop defined by the Fibre Channel (FC) Standards; and each of said communication speeds is different for each of said communication paths.

Claim 3 (canceled).

4. (currently amended) The storage unit according to claim 31,  
wherein said communication is performed through a communication path  
which is provided to connect said disk control portion and at least one of said  
disk drives in such a manner as to constitute a loop defined by the FC  
Arbitrated Loop (AL) Standards.

Claim 5 (canceled).

6. (currently amended) The storage unit according to claim 51,  
wherein said communication is performed through a communication path  
provided to connect said disk control portion and at least one of said disk  
drives in such a manner as to constitute a loop defined by the FC-AL  
Standards.

7. (currently amended) The storage unit according to claim 51,  
wherein: said charge quantity variation portion comprises a charging portion  
for charging said charge accumulation portion; and  
said charge quantity variation suppression portion comprises:  
a pulse deviation signal generation portion for generating a pulse  
deviation signal having its phase as shifted with respect to that of said pulse  
signal by certain time; and  
a discharging portion for discharging said charge accumulation portion  
only in a period when there is a potential difference between said pulse signal  
and said pulse deviation signal.

8. (currently amended) The storage unit according to claim 1, further comprising:

~~a generation portion for generating a clock signal by using a pulse signal transferred for communication between said disk control portion and said disk drives;~~

~~— a communication specifications decision portion for deciding whether said pulse signal satisfies predetermined communication specifications, when said pulse signal is read in a period of said clock signal;~~

~~— a frequency division portion for dividing a frequency of said clock signal in accordance with a result of said decision; and~~

~~— a synchronization portion for synchronizing said pulse signal with said clock signal having said divided frequency.~~

9. (previously presented) The storage unit according to claim 8, wherein said communication is performed through a communication path which is provided to connect said disk control portion and at least one of said disk drives in such a manner as to constitute a loop defined by the FC-AL Standards.

10. (previously presented) A circuit for shaping a communication signal in a storage unit according to claim 1, comprising:  
a generation portion for generating a clock signal by using a pulse signal transferred communication between said disk control portion and said disk drives;

an identification portion for identifying a frequency of said pulse signal;  
a frequency division circuit for dividing a frequency of said clock signal  
at a frequency division ratio that corresponds to a frequency of said pulse  
signal; and  
a synchronization portion for synchronizing said pulse signal with said  
clock signal having said divided frequency.

11. (original) The circuit according to claim 10, wherein said  
identification portion comprises:

a charge accumulation portion for outputting a voltage that corresponds  
to a quantity of charge accumulated therein;

a charge quantity variation portion for varying said quantity of said  
charge accumulated in said charge accumulation portion, at a certain variation  
rate;

a charge quantity variation suppression portion for inhibiting said  
variation only during a certain lapse of time each time a signal level of said  
pulse signal is switched;

a signal output portion for outputting a signal that corresponds to  
whether said voltage output from said charge accumulation portion satisfies a  
criterion;

a time measurement portion for measuring a lapse of time that has  
elapsed since said quantity of said charge accumulated in said charge  
accumulation portion started to vary; and

a frequency identification portion for identifying said frequency based  
on said lapse of time from a moment when said quantity of said charge

started to vary to a moment when said signal that indicates that said voltage of said charge accumulation portion satisfies said criterion was output.

12. (currently amended) The circuit according to claim 11, wherein:

    said charge quantity variation portion comprises a charging portion for charging said charge accumulation portion; and

    said charge quantity variation suppression portion comprises:

        a pulse deviation signal generation portion for generating a pulse deviation signal having its phase as shifted with respect to that of said pulse signal by certain time; and

        a discharging portion for discharging said charge accumulation portion only in a period when there is a potential difference between said pulse signal and said pulse deviation signal.

13. (previously presented) A circuit for shaping a communication signal in a storage unit according to claim 1, comprising:

    a generation portion for generating a clock signal by using a pulse signal transferred communication between said disk control portion and said disk drives;

    a communication specifications decision portion for deciding whether said pulse signal satisfies specifications of said communication, when said pulse signal is read in a period of said clock signal;

    a frequency division portion for dividing a frequency of said clocks signal in accordance with a result of said decision; and

a synchronization portion for synchronizing said pulse signal with said clock signal having said divided frequency.